Sai Kaushik S

Hardware Enthusiast

Sai Kaushik S
101, 2nd Main, Subbanna Garden,
Vijayanagar, Bangalore, KA - 560 040

+91 95917 16202
saikaushik609@gmail.com | ced18i044@iiitdm.ac.in
LinkedIn Profile | Github Profile | Personal Website

Skills

C, C++, Python, Verilog, Bluespec SystemVerilog
Problem Solving, Leadership skills

Education

Indian Institute of Information Technology, Design & Manufacturing, Kancheepuram, Chennai, Dual Degree (B. Tech + M. Tech) Computer Science and Engineering
JULY 2018 - PRESENT, CHENNAI

CGPA: 8.79/10

VVS Sardar Patel PU College, Class 12 (Karnataka State Board) PCME
JULY 2016 - APRIL 2018, BANGALORE

Percentage: 93.33%

Narayana e-Techno School, Class 10 (CBSE Board)
JULY 2015 - APRIL 2016, BANGALORE

CGPA: 10/10

Projects

Lorenz Attractor Parallelization Algorithm

C program for visualization of Lorenz Attractor using OpenMP, MPI, CUDA C/C++ and OpenGL.

VLIW Architecture Simulation

A python-verilog program that simulates the working of VLIW architecture.

Key Distribution Center (Kerberos)

A multi-threaded GUI application for a secure client-server communication using sockets and PyQt5.

Netlist Viewer and Simulator .v .vm

A python program that generates a graph from an input verilog .v file, or verilog netlist .vm file.

Awards

Participated in Swadeshi Microprocessor Challenge 2020.

Secured 93.5 percentile in GATE CS 2021